

February 1984 Revised February 1999

MM74HC4020 • MM74HC4040 14-Stage Binary Counter • 12-Stage Binary Counter

General Description

The MM74HC4020, MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4020 is a 14 stage counter and the MM74HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2-6V
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

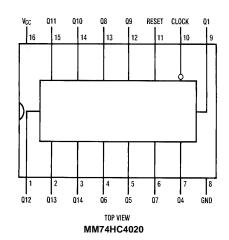
Ordering Code:

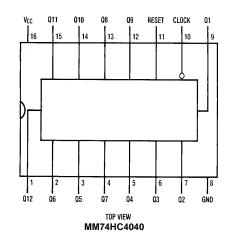
Order Number	Package Number	Package Description
MM74HC4020M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4020SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4020MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4020N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC4040M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4040SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4040MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4040N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

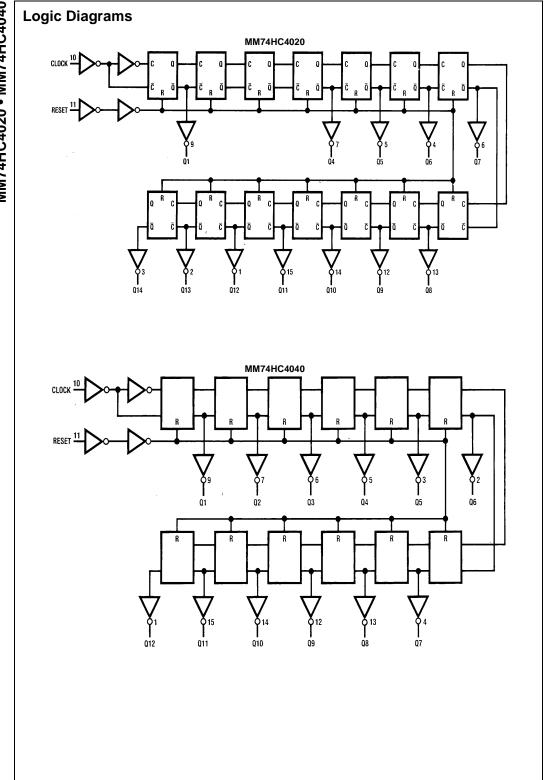
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP







Absolute Maximum Ratings(Note 1)

(Note 2)

-0.5 to $+7.0$ V
-1.5 to $V_{CC} + 1.5V$
-0.5 to V_{CC} $+0.5V$
±20 mA
±25 mA
±50 mA
-65°C to +150°C
600 mW
500 mW
260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage	0	V_{CC}	V
(V_{IN}, V_{OUT})			
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Vcc	$T_A =$	25°C	$T_A = -40 \text{ to } 85^{\circ}\text{C}$	$T_A = -55$ to 125°C	Units
Symbol			•cc	Тур	Guaranteed Limits			Units
V _{IH}	Minimum HIGH Level Input		2.0V		1.5	1.5	1.5	V
	Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level Input		2.0V		0.5	0.5	0.5	V
	Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level Output	$V_{IN} = V_{IH}$ or V_{IL}						
	Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level Output	$V_{IN} = V_{IH}$ or V_{IL}						
	Voltage	$ I_{OUT} \leq 20~\mu A$	2.0V	0	0.1	0.1	0.1	V
1			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μΑ
I _{CC}	Maximum Quiescent Supply	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μΑ
	Current	$I_{OUT} = 0 \mu A$						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency		50	30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t _{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t _{REM}	Minimum Reset Removal Time		10	20	ns
t _W	Minimum Pulse Width		10	16	ns

Note 5: Typical Propagation delay time to any output can be calculated using: tp = 17 + 12(N-1) ns; where N is the number of the output, Q_W, at V_{CC} = 5V.

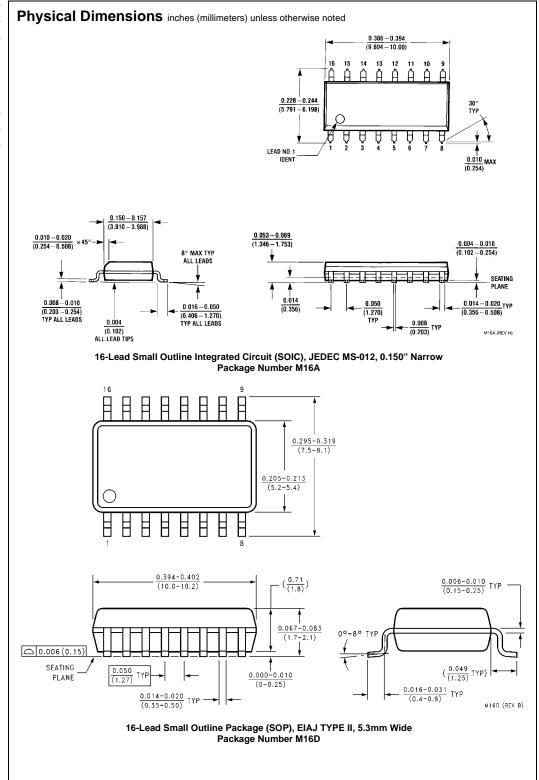
AC Electrical Characteristics

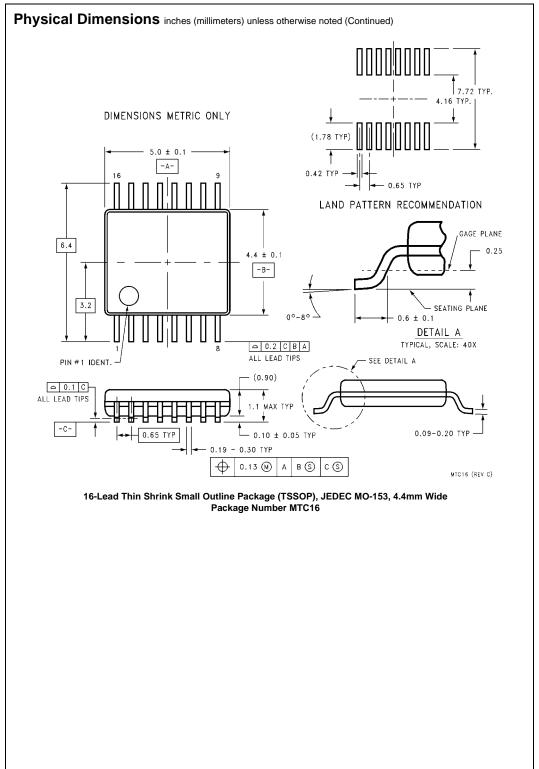
 V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_{\rm f}$ = $t_{\rm f}$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		$T_A = -40 \text{ to } 85^{\circ}\text{C}$	$T_A = -55$ to $125^{\circ}C$	Units
Symbol			•66	Typ Guaranteed Limits			Units	
f _{MAX}	Maximum Operating		2.0V	10	6	5	4	MHz
	Frequency		4.5V	40	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	80	210	265	313	ns
	Delay Clock to Q ₁		4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
T _{PHL} , t _{PLH}	Maximum Propagation		2.0V	80	125	156	188	ns
	Delay Between Stages		4.5V	18	25	31	38	ns
	from Q _n to Q _{n+1}		6.0V	15	21	26	31	ns
t _{PHL}	Maximum Propagation		2.0V	72	240	302	358	ns
	Delay Reset to any Q		4.5V	24	48	60	72	ns
	(4020 and 4040)		6.0V	20	41	51	61	ns
t _{REM}	Minimum Reset		2.0V		100	126	149	ns
	Removal Time		4.5V		20	25	50	ns
			6.0V		16	21	25	ns
t _W	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t _{TLH} , t _{THL}	Maximum		2.0V	30	75	95	110	ns
	Output Rise		4.5V	10	15	19	22	ns
	and Fall Time		6.0V	9	13	16	19	ns
t _r , t _f	Maximum Input Rise and				1000	1000	1000	ns
	Fall Time				500	500	500	ns
					400	400	400	ns
C _{PD}	Power Dissipation	(per package)		55	1			pF
	Capacitance (Note 6)							
C _{IN}	Maximum Input			5	10	10	10	pF
	Capacitance							

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.

Timing Diagram





Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)**16 15 14 13 12 11 10 9** 16 15 INDEX AREA 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 _ OPTION 01 OPTION 02 $\frac{0.065}{(1.651)}$ $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 4° TYP 0.300 - 0.320 OPTIONAL (7.620 - 8.128) 0.145 - 0.200 $\overline{(3.683 - 5.080)}$ 95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 90° ± 4° TYP 0.020 $\frac{0.280}{(7.112)}$ MIN (0.508)0.125 - 0.150 (3.175 - 3.810) (0.762 ± 0.381) 0.014 = 0.023 (0.356 = 0.584) 0.100 ± 0.010 (0.325 +0.040 -0.015 (2.540 ± 0.254) 0.050 ± 0.010 N16E (REV F) TYP (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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